AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph beginning at page 1, line 10, as follows:

This application is <u>a</u> counterpart of Japanese patent <u>application</u> applications, Serial Number 345641/2002, filed November 28, 2002, the subject matter of which is incorporated herein by reference.

Please amend the paragraph beginning at page 2, line 22, as follows:

With an object of overcoming such a problem, there has since been proposed, for example, a semiconductor device (CSP) wherein connecting wiring is formed so as to extend from the surface of a semiconductor chip, on which an integrated circuit containing a photoreception region is formed, to a side face or the back face thereof in JP-A-2002-198463, A. With the semiconductor device (CSP), since the connecting wiring is formed so as to extend from the surface of the semiconductor chip to the side face or the back face thereof, the semiconductor device can be surface mounted on, for example, a mounting board, and so forth such that the surface of the semiconductor device, with a photoreception region (integrated circuit) formed thereon, faces outside so as to enable photoreception, thereby attaining ultracompact mounting as a wafer level CSP.

Please amend the paragraph beginning at page 3, line 16, as follows:

However, it is to be pointed out that although the proposal described above has attained ultra-compact mounting, only an insulator layer is provided on the integrated circuit (photoreception region), although a form wherein a protection film is additionally formed on the integrated circuit is also disclosed, insufficiency in respect of durability still remains at present

when taking into consideration the fact that the same is handled as one component as packaged.[[,]]

Please amend the paragraph beginning at page 4, line 20, as follows:

Figs. 1(A) and 1(B) are Fig. 1 is a schematic illustrations illustration showing the configuration of a first embodiment of a semiconductor device according to the invention, where and Fig. 1 (A) is a plan view, and Fig. 1 (B) is being a sectional view;

Please amend the paragraph beginning at page 5, line 9, as follows:

Figs. 5(A) and 5(b) are Fig. 5 is a sectional views view showing another example of a method of sealing with a sealing resin in the semiconductor device according to the first embodiment, where and Fig. 5 (A) is a sectional view, and Fig. 5 (B) is being a plan view;

Please amend the paragraph beginning at page 5, line 12, as follows:

Figs. 6(A) and 6(B) are Fig. 6 is a sectional views view showing still another example of a method of sealing with a sealing resin in the semiconductor device according to the first embodiment, where and Fig. 6 (A) is a sectional view, and Fig. 6 (B) is being a plan view;

Please amend the paragraph beginning at page 5, line 16, as follows:

Figs. 7(A) and 7(B) are Fig. 7 is a schematic illustration showing the configuration of a second embodiment of a semiconductor device according to the invention, where and Fig. 7 (A) is a plan view, and Fig. 7 (B) is being a sectional view;

Please amend the paragraph beginning at page 5, line 19, as follows:

Figs. 8(A) and 8(B) are Fig. 8 is a schematic illustration illustration showing the configuration of a third embodiment of a semiconductor device according to the invention, where and Fig. 8 (A) is a plan view, and Fig. 8 (B) is being a sectional view;

Please amend the paragraph beginning at page 5, line 22, as follows:

Figs. 9(A) and 9(B) are Fig. 9 is a schematic illustrations illustration showing the configuration of a fourth embodiment of a semiconductor device according to the invention, where and Fig. 9 (A) is a plan view, and Fig. 9 (B) is being a sectional view;

Please amend the paragraph beginning at page 6, line 14, as follows:

Embodiments of a semiconductor device according to the invention are described hereinafter with reference to the accompanying drawings. Parts having the same functions in effect are denoted by like reference numerals throughout the figures, omitting description thereof in some cases.

Please amend the paragraph beginning at page 6, line 19, as follows:

Figs. 1(A) and 1(B) are Fig. 1 is a schematic illustrations illustration showing the configuration of a first embodiment of a semiconductor device according to the invention, where and Fig. 1 (A) is a plan view, and Fig. 1 (B) is being a sectional view. Figs. 2 (A) through 2 (J) are schematic sectional views for illustrating a method of manufacturing the semiconductor device according to the first embodiment.

Please amend the paragraph beginning at page 7, line 2, as follows:

A semiconductor device 100 shown in Figs. 1(A) and 1(B) Fig. 1 has a semiconductor chip 10 on which surface there is formed an integrated circuit (referred to as a photoreception region in some cases hereinafter because the integrated circuit herein contains a photoelectric converter: a region denoted by reference numeral 12 in the figure) containing a photoelectric converter (solid state image sensor such as, for example, a CCD (charge-coupled device), CMOS (Complementary Metal-Oxide-Semiconductor) sensor, photodetector, etc.). Electrode pads

Electrodes 14 electrically continuous with the integrated circuit are formed on top of the semiconductor chip 10, and an insulator film (for example, a passivation film) 16 and a protection film (for example, a polyimide film) 18 are sequentially formed in part of the semiconductor chip 10, other than parts where the electrode pads electrodes 14 are provided.

Please amend the paragraph beginning at page 7, line 15, as follows:

Further, with the semiconductor device 100, there are formed a redistribution wiring layer 20 extended from the respective <u>electrode pads</u> <u>electrodes</u> 14, and bumps 22 for electrical connection with pads 24 for external connection, respectively, on the redistribution wiring layer 20. The bumps 22 are formed in the vicinity of the periphery of the integrated circuit, and are provided with a step 22a at respective tips thereof while the redistribution wiring layer 20 and the outer periphery of bumps 22, on the semiconductor chip 10, are sealed with a sealing resin 26 so as to have an opening over an integrated circuit surface. A light-transmitting cap 30 is engaged with the step 22a at the respective tips of the bumps 22, and is disposed in such a way as to cover the opening in the sealing resin 26.

Please amend the paragraph beginning at page 8, line 14, as follows:

Now, a process of manufacturing the semiconductor device 100 shown in Figs. 1(A) and 1(B) Fig. 1 is described hereinafter by way of example.

Please amend the paragraph beginning at page 8, line 16, as follows:

First, there is prepared a wafer 32, on which an integrated circuit of an element serving as a semiconductor chip 10 is formed, after evaluation of electrical characteristics thereof {Fig. 2 (A)}. The protection film 18 film18 is applied to portions of the wafer 32, where the insulator film over the electrode pads electrodes 14 is removed, by the spin coater method, and so forth, and the protection film 18 film18 is etched by subjecting the same to exposure using a mask for contact with the respective electrode pads electrodes 14 {Fig. 2 (B)}. The redistribution wiring layer 20 as a base for forming wiring to be extended from the respective electrode pads electrodes 14 and forming the bumps 22 is formed by sputtering, plating, and so forth {Fig. 2 (C)}.

Please amend the paragraph beginning at page 12, line 16, as follows:

Figs. 7(A) and 7(B) are Fig. 7 is a schematic illustration illustration showing the configuration of a second embodiment of a semiconductor device according to the invention, where Fig. 7 (A) is a plan view, and Fig. 7 (B) is a sectional view.

Please amend the paragraph beginning at page 12, line 19, as follows:

The semiconductor device according to the second embodiment is the same in configuration as the semiconductor device according to the first embodiment except that a

protection film 18 having an opening 18a over an integrated circuit (photoreception region) is provided. As a method of providing the protection film 18 film 18 with the opening 18a, there are available a method of selectively forming the protection film 18 film 18 with the opening 18a, a mask at the time of forming the protection film 18 film 18 film 18 (refer to Fig. 2 (B)) in the process of manufacturing the semiconductor device as described in the first embodiment, thereby defining the opening 18a, a method of forming the redistribution wiring layer 20 (refer to Fig. 2 (C)), and subsequently, defining the opening 18a by etching a portion of the redistribution wiring layer 20, in the integrated circuit forming region, by photolithographic techniques, and so forth.

Please amend the paragraph beginning at page 13, line 10, as follows:

When resin films having high dielectric constant (in the case of the first embodiment, the insulator film 16 and the protection film 18 film18) exist in the vicinity of a circuit, electric current normally has difficulty in flowing through the circuit. The reason for this is because the resin films (the dielectric constant of resin is normally about 4) having high dielectric constant block a magnetic field generated upon electric current flowing through the circuit, resulting in an increase in resistance of the circuit.

Please amend the paragraph beginning at page 13, line 17, as follows:

With the present embodiment, therefore, a portion of the protection <u>film 18</u> film18 among the resin films existing in the vicinity of integrated circuit, contributing to an increase in resistance, is removed, thereby causing the dielectric constant thereof to approach that of air, that is, 1, as much as possible, so that the semiconductor device can better cope with high speed RF.

Please amend the paragraph beginning at page 14, line 2, as follows:

Figs. 8(A) and 8(B) are Fig. 8 is a schematic illustration showing the configuration of a third embodiment of a semiconductor device according to the invention, where Fig. 8 (A) is a plan view, and Fig. 8 (B) is a sectional view.

Please amend the paragraph beginning at page 14, line 5, as follows:

With the semiconductor device according to the third embodiment, a light-transmitting cap 30 is made up of a portion of a wiring board 30a, and a cap 30b assembled into the central part of the wiring board 30a. Wiring 30c causing electrical electrically continuity between the top surface and the back side by forming a through hole or the like for electrically connecting respective bumps 22 with respective pads 24 is provided on the periphery of the wiring board 30a. The wiring 30c is formed in the same wiring pattern as that for an ordinary printed wiring board. Further, the wiring board 30a may be of a multilayer multiplayer wiring structure. The light-transmitting cap 30 can be made with ease by, for example, defining an opening at the central part of the wiring board 30a provided with any suitable wiring pattern, and provided with a protection film of a solder resist, and so forth, formed thereon, and by fitting the cap 30b into the opening.

Please amend the paragraph beginning at page 15, line 19, as follows:

Figs. 9(A) and 9(B) are Fig. 9 is a schematic illustration showing the configuration of a fourth embodiment of a semiconductor device according to the invention, where Fig. 9 (A) is a plan view, and Fig. 9 (B) is a sectional view.